ENABLING TECHNOLOGIES FOR SOFTWARE DEFINED RADIO TRANSCEIVERS.

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ABSTRACT:

This paper discusses the design considerations related to the transceiver hardware elements within a Software Defined Radio (SDR). Receiver architectures are reviewed and the viability of manufacturing these in the short to medium term is considered. The filtering functions required for a conventional receiver are examined, and the problems associated with implementation of these filters within a SDR receiver discussed, including that of image filtering. Receiver linearity requirements are evaluated in terms of typical user applications and it is shown that these will be onerous in the case of a SDR receiver. A novel technique for mixer linearisation is presented as a potentially enabling element within a re-configurable transceiver and some initial performance results are reported. The possibility of constructing an electronically tunable preselection filter using Micro Electromechanical Systems (MEMS) technology is examined. Some simulation and prototype measurement results are presented.

INTRODUCTION

An ideal SDR should have the ability to transmit and receive signals which adhere to any radio standard - both current and future generations. Clearly, meeting these open-ended expectations is impossible. For the purposes of this paper, we will consider a SDR as being able to be reconfigured to function with any of the major European air interface standards relating to 2G Mobile Phones (GSM900 and GSM1800), Cordless Phones (DECT), 3G Mobile Phones (UMTS - FDD & TDD), Radio Personal Area Networks (Bluetooth) and Radio Local Area Networks (HIPERLAN/2 and the IEEE802.11 family).

For total flexibility, a SDR receiver should have the Analogue to Digital Converter (ADC) placed adjacent to the antenna. The problems associated with this "direct sampling" of the RF signal are discussed shortly.

RECEIVER ARCHITECTURE

In this section of the paper we discuss numerous candidate receiver architectures.

One possible architecture is direct digitization of the signal, that is, the direct sampling of the RF signal to generate a digital IF signal The basic constraint of the sampling theorem is that the signal being processed must be sampled at a rate equal to twice its bandwidth. The analogue channel of the sampler must have sufficient bandwidth to accommodate all desired signals. Figure 1 shows a possible direct digitization architecture.

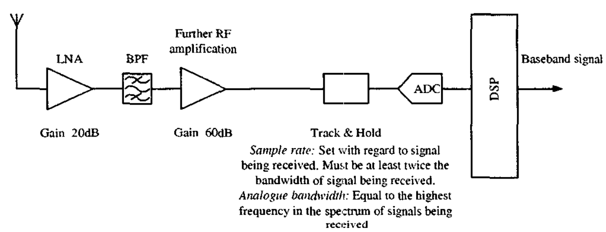

Figure 1 Direct digitization

This technique is known as "under sampling" as the sampling frequency is less than the center frequency of the signal being sampled. It will function provided that the signal incident on the "track and hold " circuit is narrow band. This implies that the band pass filter that precedes the "track and hold" circuit must have a center frequency equal to the center frequency of the air interface standard being sampled and a bandwidth equal to the complete bandwidth of that standard. This filter is in effect an anti-ailiasing filter. If this filter is omitted[1], the whole of the spectrum present on the antenna will be mixed down to IF and our required signal will be lost due to ailiasing. So that, although direct digital sampling is theoretically possible, without filters to define the channel that we are sampling, then all the signals that reach the antenna will be

[1] We would like to omit this filter as its presence detracts considerably from the flexibility of the receiver.

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digitally converted to a composite baseband signal. This will make it impossible to recover the wanted signal. The easiest way to resolve this problem is to use at least one stage of analogue signal processing to convert the signal to an IF frequency. This leads to the combination of analogue RF and digital IF stages that will be discussed soon.

Another problem associated with under-sampling is that of sampling jitter. Any deviation of the sampling clock signal is magnified by the order of "under sampling" taking place.

ZERO IF ARCHITECTURE

An alternative to direct digitization for SDR has been the zero IF architecture. This approach is potentially attractive since it does not require any image filtering (as image cancellation is implicit in the architecture), and the hardware is considerably simplified. A zero IF receiver is shown in Figure 2. Unfortunately, apart from the above potential benefits, there are several major pitfalls with this architecture.

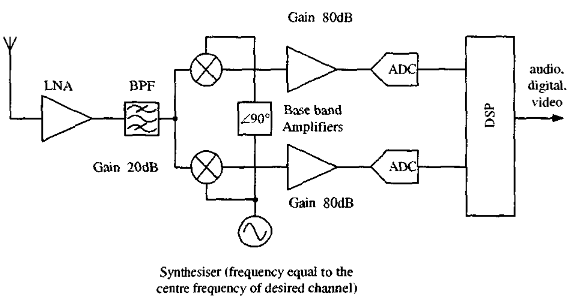

Figure 2 Zero IF receiver

The principal disadvantages (and there are others) of zero IF are:

(i) The Local Oscillator (LO) must produce two signals that are in precise phase quadrature, and precise amplitude balance, over the whole frequency range covered by the receiver.

(ii) It is possible for the local oscillator signal to "reflect off" the time varying impedance of the antenna. When this signal mixes with itself, a slowly time varying signal (near DC) is detected. This signal can be substantially greater than the wanted signal and it will result in large DC offsets.

It is necessary for the LO to maintain accurate amplitude balance and phase quadrature to not only to demodulate modern digital modulation formats, but also to provide the necessary image rejection. With a zero IF stage, this wide-band quadrature local oscillator must be implemented in the RF circuitry. Given the tendency for RF circuits to drift with time and temperature, maintaining this performance, even at a spot frequency, will be extremely difficult.

A superheterodyne receiver is shown in Figure 3. The major advantages of this structure is that the conversion from a real to a complex signal is done at one fixed frequency, and therefore a phase quadrature, amplitude balanced local oscillator, is only required at a single frequency and may be implemented in DSP as indicated in Figure 3.

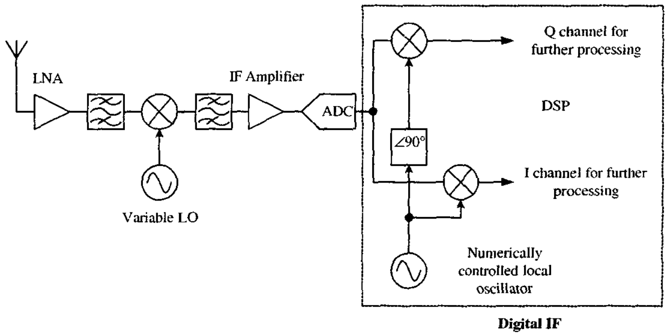

Figure 3 Superheterodyne receiver

The chief disadvantage of this architecture is that complexity is high due to the various mixing, filtering and amplifying stages, and implementation in the form of an integrated circuit is difficult.

Although the stage of Figure 3 only shows 2 explicit down-conversions (one in the RF hardware and the other in the DSP (Digital Signal Processing)), further conversions can be done in the DSP. It can be seen that this type of architecture represents a practical implementation of the direct digitization stage discussed previously.

FILTER FUNCTIONS WITHIN A CONVENTIONAL RECEIVER

In any radio receiver that employs a superheterodyne architecture, filters are required to perform three functions.

- Band-limit the signal to the frequency of interest. This function is often referred to as "channelisation" and is often implemented within the digital baseband processing of the receiver.
- Suppression of the image signal with respect to the wanted signal. This function is performed at the first opportunity in the receiver chain.
- Suppression of out-of-band "blocker" signals to prevent them generating sufficient "in-band" power to interfere with the wanted signal.

It should be noted that if the receiver components were perfectly linear, then it would not be possible for out-of-band signals to generate in-band products and a filter to achieve this function would not be needed. In practice, some degree of non-linearity exists in all the amplifiers and mixers that make up the receiver chain. This means that some degree of bandwidth constriction is essential at an early stage in the receiver.

DEVICE LINEARITY

A useful measurement of distortion for receiver design purposes is *Third Order Intercept (TOI)*. *TOI* is the value of input (or output power) at which the third order intermodulation distortion product rises to meet the fundamental output power.

Blocker specifications are an important factor in determining the allowed distortion performance of a receiver. Reference to these specifications for a GSM system shows that if the receiver has a 5MHz RF bandwidth to accommodate the 5 MHz channel of UMTS, then any blocker within ±2.5MHz of the center frequency may introduce distortion products into the wanted GSM channel. Blockers at these frequencies are allowed to be up to –23dBm. Calculations based on the minimum specified GSM signal and the maximum allowable "in-band" interference due to the blockers will show that the minimum input TOI will be +20.5dBm. This is an onerous linearity specification and obtaining devices (mixers and amplifiers) with this specification is currently not possible, when considering cost and power-consumption issues.

We can infer from this result, that the receiver of a SDR should be extremely linear. In general, for best overall distortion performance, the components where the signal is at its highest power levels require the best distortion performance.

The University of Bristol is currently active in several research projects on linearising receiver components (as opposed to more conventional work on linearising PAs – see for example, reference [1]). Reference [2] discusses the linearisation of wide-band RF receiver amplifiers.

MIXER LINEARISATION

The distortion performance of a mixer can be a bottle neck in the overall system distortion performance, because the mixer is usually located within the receiver, at relatively high signal power levels (compared to the LNA). It is generally hard to achieve an improved *TOI* figure for a mixer, whilst at the same time not increasing the noise floor. This section will report on a new technique that achieves an increase in *TOI* without a corresponding degradation of the noise figure. Some practical results will also be presented.

Feedforward has been previously applied to amplifiers yielding significant reduction in Inter Modulation Distortion (IMD) products at the output. Applying feedforward to mixers necessitates a different approach, since frequency translation occurs making the generation of the reference and error signals difficult. Considering a receiver, the reference (undistorted clean signal at RF input) and the output signals where the IMD products exist (at IF) are at different frequencies, and thus comparing them is not possible.

Current mixer linearisation techniques ([3]) are unable to simultaneously offer a large dynamic range, low noise and suppress IMD. Figure 4 shows a novel receiver architecture in order to overcome these shortcomings (for more details see [4]). The system will be explained considering a receiver application downconverting RF to IF however, it can also be applied to a transmitter.

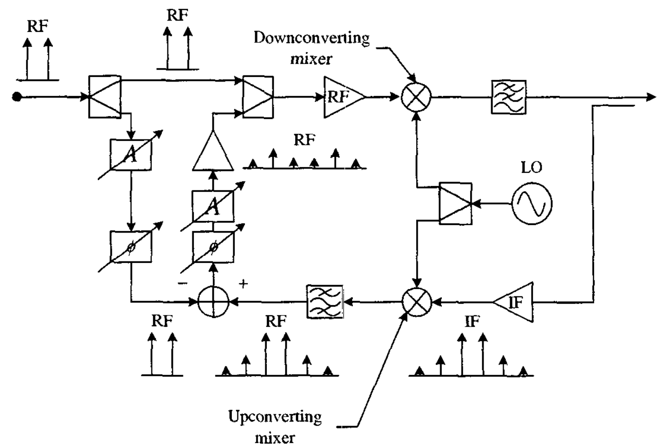

Figure 4 Frequency retranslation applied to a receiver

The distorted output of the downconverting mixer at IF is coupled, amplified, and *frequency retranslated* back to RF by the upconverting mixer and filtered to remove unwanted image signals. The clean (reference) signal at the receiver front-end is also coupled and added in anti-phase to the frequency retranslated IF output (which is now at RF) with correct amplitude. This process cancels the fundamental signals and produces an error signal including only the IMD products. This error signal is then combined with the received RF input signal with correct amplitude and phase relation to *predistort* the saturated downconverting mixer. This provides suppression of the IMD without affecting the fundamental signal level, if the signal cancellation is also correctly optimized. The linearity of the second (upconverting) mixer is not critical since it is not frequency translating the reference signal, but the already distorted IF output. Here, signal cancellation is the vector addition of the reference and frequency retranslated IF output, with system performance critical on the optimization of this parameter, in common with other feedforward linearisation architectures. In a practical application an adaptive control scheme would be necessary in order to maintain system performance with changing circuit parameters.

A prototype demonstrator has been constructed and some measurements made. A two-tone-test was applied at 920MHz with Δf = 100kHz, the RF downconverted to an IF at 160MHz. After applying the frequency retranslation technique Figure 5 shows 24dB *IM3* suppression. Increasing the frequency separation degrades the signal cancellation and hence the *IM3* suppression.

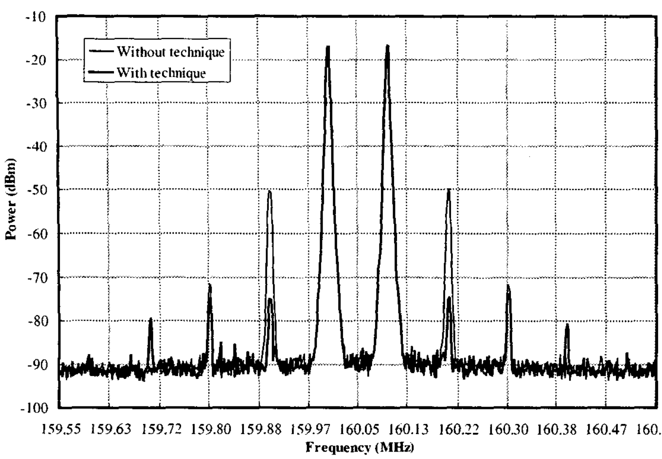

Figure 5 Two-tone-test showing 24dB *IM3* improvement.

Further results have been taken (see [4]) to suggest that this technique is a real contribution to receiver linearity and a useful SDR architecture.

IMAGE SIGNALS

Image signals are controlled in conventional receivers via the use of preselect filters. Switchable or electronically tunable filters will be needed to perform this function in a superheterodyne SDR. Simple microwave tuned filters have traditionally relied on varactor tuning. To meet the linearity requirements of a re-configurable receiver however, new approaches such as tunable dielectric properties, or the use of MEMS switching are likely to be needed.

The options for the design of a flexible preselect filter is at present limited to realization as either a distributed component design, or as a MMIC.

There have been a number of tunable MMIC filter designs reported in the literature (e.g. [5]). MMIC designs tend to suffer from poor TOI performance. This has two causes. First it occurs because a varactor is often used to tune the device, and second, a nonlinear active device is often used to compensate losses in the filter components[2].

Distributed component filters are a second option. The design problem to be solved is how they might be tuned. A number of suggestions follow.

- Varactor diode tuning at some strategic point on the filter structure. This technique has been dismissed previously because of the nonlinearities associated with the tuning elements.
- Constructing the filter on a substrate, whose dielectric constant could be electrically varied. This is a possibility, which is yet to be actively pursued.
- Switching parts of the transmission line so that the physical characteristics of the filter structure could be changed

Switching the component parts of a filter, in and out of circuit, using Micro Electro-Mechanical Structures (MEMS) seems to offer an alternative solution The use of Electro-mechanical switches will mean that the filter is composed entirely of linear components, and therefore the dynamic range of the filter should not be compromised. The major problem with electrically switching a filter is to preserve the filter geometry as the center frequency is translated, whilst at the same time utilizing an essentially simple switching arrangement.

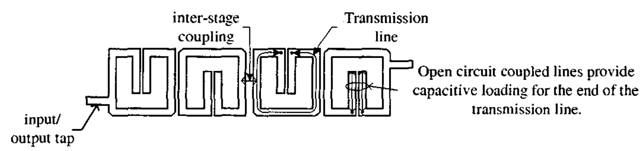

Figure 6 Hairpin filter structure

At the time of writing, the simplest arrangement for tuning the filter characteristic via this method would appear to be the modified hairpin structure shown in Figure 6. This filter has a coupled line, which provides a capacitive load at the end of a microstrip line. Such capacitive loading effectively shortens the length of transmission line required to form a filter resonator (normally half a wavelength). Filters that employ technique are known as "slow-wave filters". References [6] to [8] give design information for this filter architecture. Inter-stage transformer action is bought about by edge coupling of the "U-shaped" structures. Tuning of this filter using MEMS can potentially be achieved by shortening the capacitive loading coupled line, as shown in Figure 7.

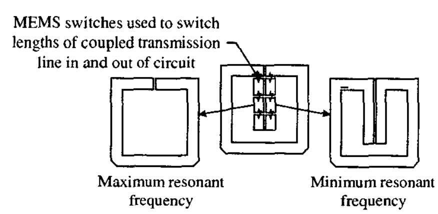

Figure 7 Switching filter center frequency using MEMS

A simple filter of this type has been simulated on MOMENTUM. MOMENTUM is the electromagnetic simulator associated with Agilent Technologies' ADS (Advanced Design Systems) package. The results of this simulation are shown in Figure 8. The filter has been simulated with various lengths of coupled line that load the hairpin. The design bandwidth for the filter is 5%.

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[2] By introducing, for example, negative resistance across an inductor.

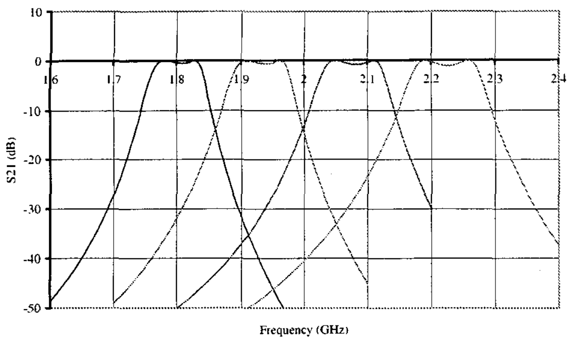

Figure 8 Simulated response of MEMS-tuned hairpin filter

Figure 9 shows the measured response of a prototype filter. Note that the pass band loss is of the order of 6dB and the response is skewed. Further work is needed but progress is encouraging.

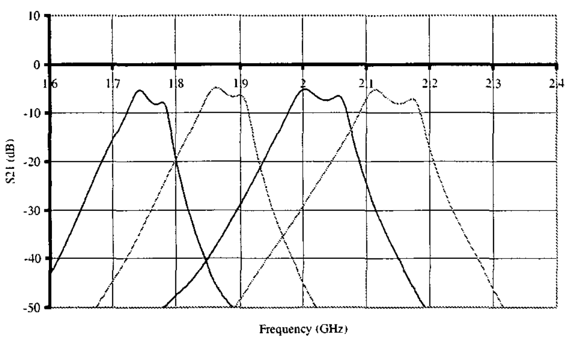

Figure 9 Measured response of MEMS-tuned hairpin filter

CONCLUSIONS

This paper has concentrated on receiver design, as it is potentially the most difficult part of a SDR design. Some of the techniques discussed however are directly applicable to transmitter design.

Possible architectures for a SDR receiver were discussed. Direct digitization was seen to be an impractical proposition at this stage. It was also concluded that Zero IF receivers have many problems, which must be solved before they are a viable architecture for use in a SDR. The superheterodyne stage is seen as the most immediately useful architecture.

The functions of filters within a receiver were briefly discussed.

The importance of device linearity in helping the re-configurable receiver meet it's blocking performance objectives was also discussed.

The paper then focused on the problem of mixer linearity, and a new linearisation technique was introduced. A hardware prototype has been constructed some results were presented.

A possible electronically tunable RF filter, using MEMS switches, was presented as a method of providing the preselect function in an SDR receiver. Some simulation and measurement results were reported.

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